

REMARKS

Applicants express appreciation to Examiner Rao for the courtesy of the Examiner Interview conducted on February 8, 2006. By this Amendment, Applicants have attempted to amend the claims in a manner that is consistent with the discussions conducted with Examiner Rao at the February 8 Interview. Nonetheless, if there are additional concerns and/or questions that the Examiner may have, then the Examiner is encourage to contact the undersigned by telephone at 202-842-8886 so that any such issues may be resolved in as efficient and expeditious manner as possible. In view of the foregoing:

Applicants have amended claim 1-4, 7-13, and 15 to differently recite the invention. Claims 17-25 are withdrawn from consideration. Claims 1-16 are pending.

In the Office Action, the Examiner rejected claims 1-13 and 15 under 35 U.S.C. § 103(a) as being unpatentable over Mattson et al. (U.S. Patent No. 6,4266,991) in view of Chappo et al. (U.S. Patent No. 6,510,195); and rejected claim 16 under 35 U.S.C. § 103(a) as being unpatentable over Mattson et al. in view of Chappo et al. and Yamanaka (U.S. Patent No. 6,372,558). Applicants traverse these objections and rejections, at least for the following reasons.

The Examiner has not applied any rejection to claim 14. Accordingly, Applicants submit that claim 14 should now be in condition for allowance.

With regard to an issue that was discussed during the February 8 interview, Applicants confirm that the recitation in independent claim 1 corresponds to the case where a thinner portion of the first conductive type semiconductor substrate exists at the location of each recessed portion (e.g., the recessed portion is an indentation rather than an opening penetrating the

substrate). Support for this recitation can be found in Applicants' specification beginning at page 4, line 15, for example. With regard to the recitation in claim 13, Applicants submit that support can be found in Applicants' specification beginning at page 10, line 16.

Further to the remarks that Applicants have provided previously, Applicants traverse the rejections applied to remaining claims 1-13, 15, and 16 at least because the applied references do not disclose or suggest any of Applicants' claimed combinations wherein said first conductive type semiconductor substrate is thinner in said recessed portions of said first conductive type substrate than in portions of said first conductive type semiconductor substrate located around said recessed portions. In connection with this point, Applicants reiterate their previous reference to Applicants' specification for background discussion relating to, but not limiting of, such claimed subject matter.

Again, in the paragraph beginning at page 4, line 4, Applicants' specification states that:

"Since the back illuminated photodiode array of the invention is provided with the second conductive type semiconductor regions at the bottom of the recessed portions formed on an opposite surface, it is possible to make a distance between the light-incident surface of the semiconductor substrates and the semiconductor regions shorter, thereby it is possible to inhibit a phenomenon that a carrier generated by incident light that undergoes recombination during a transferring process, then a higher detection sensitivity is kept on. Furthermore, the recessed portions can be formed in an array." (Underlining added.)

Then, in the paragraph beginning at page 5, line 11, Applicants' specification states that:

"More particularly, a distance between the light-incident surface and the second conductive type semiconductor region, i.e., the surface where photodiodes are arranged is determined by the thickness of the first semiconductor substrate. Since the first semiconductor substrate can be made thinner by the existence of the frame part surrounded by the recessed portions, while it keeps the mechanical strength carrier generated inside the semiconductor substrate will move at a shorter distance. Thus, the recombination of carriers are inhibited to maintain a higher detection sensitivity of the back illuminated photodiode array." (Underlining added.)

Thus, a plurality of recessed portions may be utilized to reduce the distance between the light-incident surface of the semiconductor substrates and the semiconductor regions, which in turn makes it possible to inhibit carrier recombination so as to maintain a higher detection sensitivity. And, at the same time, a frame structure surrounding the recessed portions can be configured so that the frame portion around each recessed portion is thicker than the thickness of recessed portion which it surrounds, which provides mechanical strength. In other words, the thinness of the recessed portions allows higher detection sensitivity while at the same time the thickness of the frame portion provides mechanical strength. Thus, a structure combining the two may be high in both detection sensitivity and mechanical strength.

In contrast to the subject matter recited in Applicants' independent claim 1, the applied Mattson et al. reference purportedly discloses a back illuminated photodiode (BIP) array comprising a first conductive type flat semiconductor substrate having a light-incident surface (Fig. 3). However, Applicants submit that this substrate does not have a plurality of recessed portions as recited Applicants' claim 1. Nor, as apparently recognized by the Examiner, does Yamanaka et al. make up for this deficiency.

Instead, the Examiner relies on Chappo et al. as suggesting the plurality of recessed portions. Specifically, the Examiner apparently relies on element 54 of Chappo et al. as providing the suggestion for a plurality of recesses. However, rather than being a recess, Chappo et al. indicates at column 6, line 55, that element 54 represents contact pads. Perhaps more importantly, even if element 54 of Chappo et al. would be considered to represent recesses, the recitation in Applicants' independent claim 1 would still not be met at least because combining Chappo et al. to the primary reference to Mattson et al. would simply not result in the back

illuminated photodiode array of claim 1 comprising a plurality of spatially separated second conductive type semiconductor regions, one of which is located at each bottom of said recessed portions, wherein said second conductive type semiconductor regions each individually constitute a pn junction together with said first conductive type semiconductor substrate, and wherein said first conductive type semiconductor substrate is thinner in said recessed portions of said first conductive type substrate than in portions of said first conductive type semiconductor substrate located around said recessed portions.

For at least the foregoing reasons, Applicants submit that independent claim 1, and each of the dependent claims depending therefrom, patentably distinguish over the references applied to the claims in the pending Office Action. Accordingly, reconsideration and withdrawal of all rejections set forth in the pending Office Action are respectfully requested.

CONCLUSION

In view of the foregoing, Applicants submit that the pending claims are in condition for allowance, and respectfully request reconsideration and timely allowance of the pending claims. Should the Examiner feel that there are any issues outstanding after consideration of this response, the Examiner is invited to contact Applicants' undersigned representative to expedite prosecution. A favorable action is awaited.

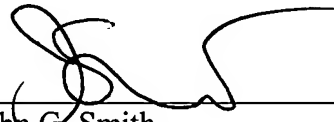
EXCEPT for issue fees payable under 37 C.F.R. § 1.18, the Commissioner is hereby authorized by this paper to charge any additional fees during the entire pendency of this application including fees due under 37 C.F.R. §§ 1.16 and 1.17 which may be required,

including any required extension of time fees, or credit any overpayment to Deposit Account No. 50-0573. This paragraph is intended to be a **CONSTRUCTIVE PETITION FOR EXTENSION OF TIME** in accordance with 37 C.F.R. § 1.136(a)(3).

Respectfully submitted,

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